Memory Managment - Part II

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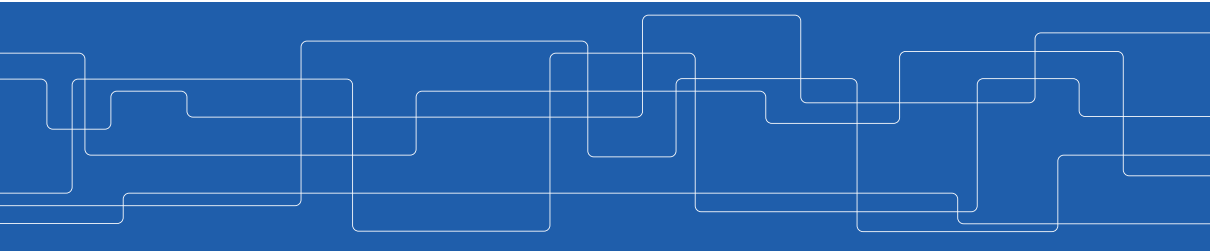
2022



Reminder

Reminder (1/3)

- External fragmentation vs. internal fragmentation

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- Compaction: shuffle memory contents to place all free memory together in one large block.

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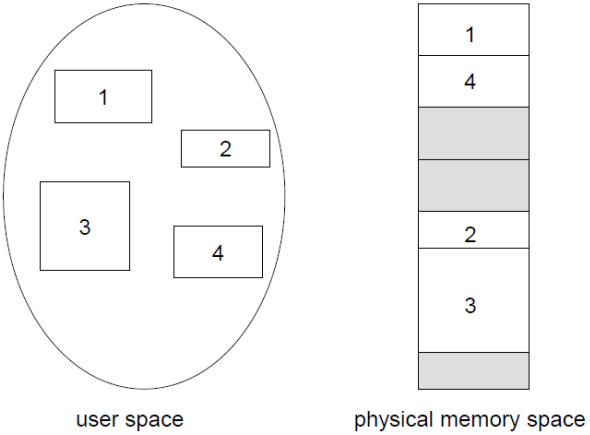
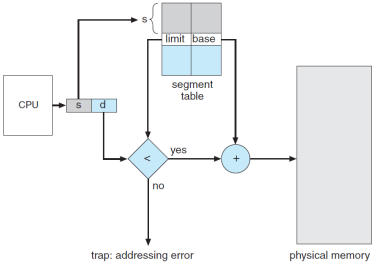
- External fragmentation vs. internal fragmentation
- Compaction: shuffle memory contents to place all free memory together in one large block.
- Other solutions:
  - Segmentation
  - Paging

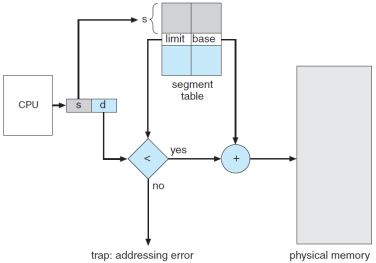
Reminder (2/3)



Reminder (3/3)


s
limit
base
segment table
CPU
s
d
<
yes
no
+
trap: addressing error
physical memory

Reminder (3/3)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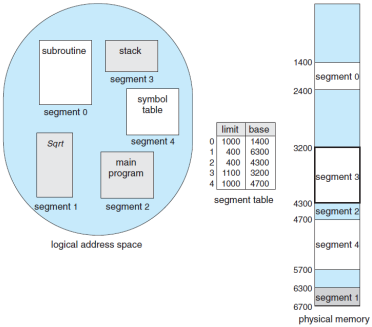
subroutine
stack
segment 3
segment 0
symbol table
segment 4
Sqrt
main program
segment 1
segment 2
logical address space
limit
base
0 1000 1400
1 400 6300
2 400 4300
3 1100 3200
4 1000 4700
segment table
1400
segment 0
2400
3200
segment 3
4300
segment 2
4700
segment 4
5700
6300
segment 1
6700
physical memory

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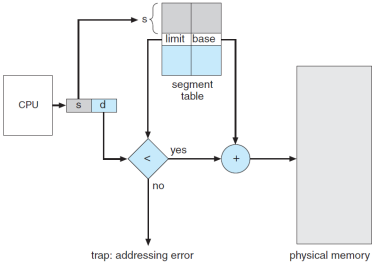
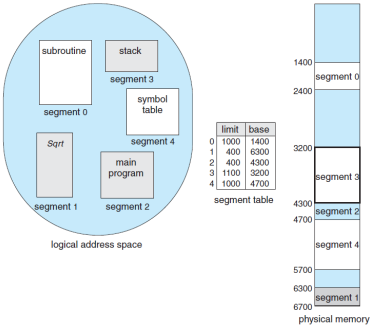
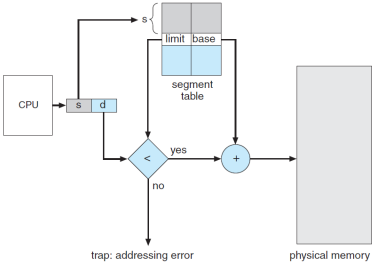
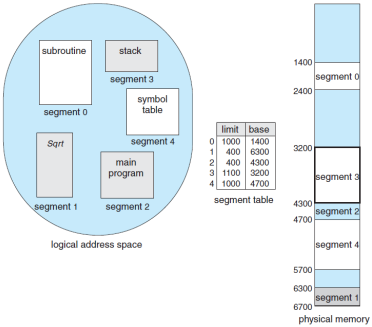




- A reference to byte 53 of segment 2:

Reminder (3/3)





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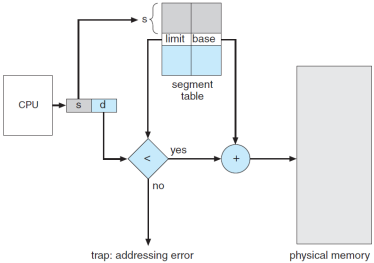
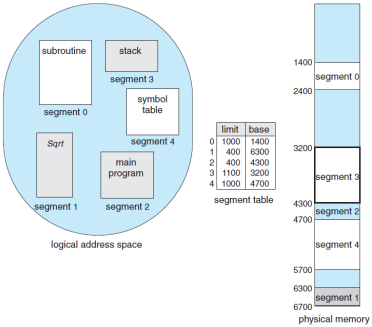
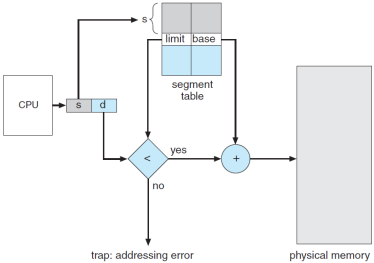
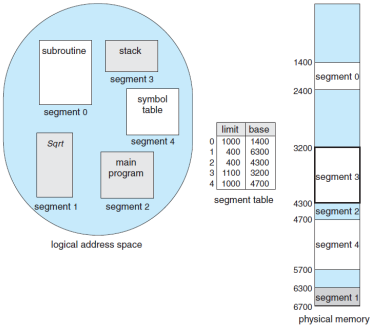




- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- A reference to byte 852 of segment 3:

Reminder (3/3)





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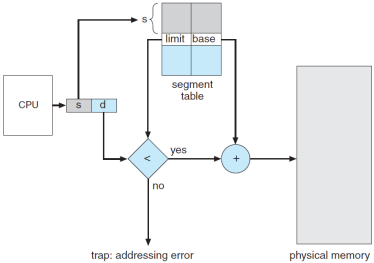

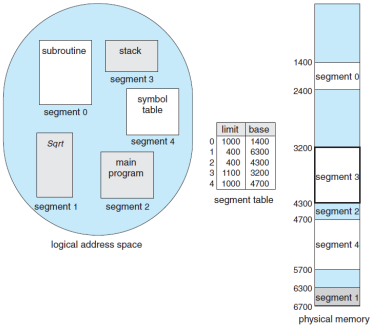

- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
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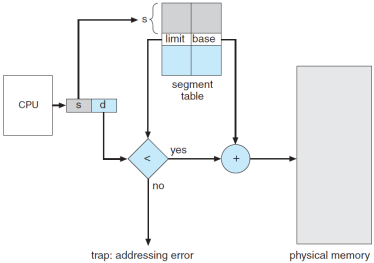

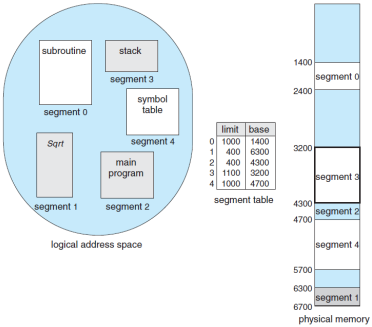

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Paging

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- Segmentation and paging, both, permit the physical address space of a process to be noncontiguous.

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- Paging avoids external fragmentation and the need for compaction, whereas segmentation does not.

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- Divide physical memory into fixed-sized blocks called frames.
  - Size is power of 2, between 512 bytes and 16 Mbytes.
- Divide logical memory into blocks of same size called pages.

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- Keep track of all free frames.
- To run a program of size N pages, need to find N free frames and load program.
- Set up a page table to translate logical to physical addresses.
- Still have internal fragmentation.

Address Translation Scheme

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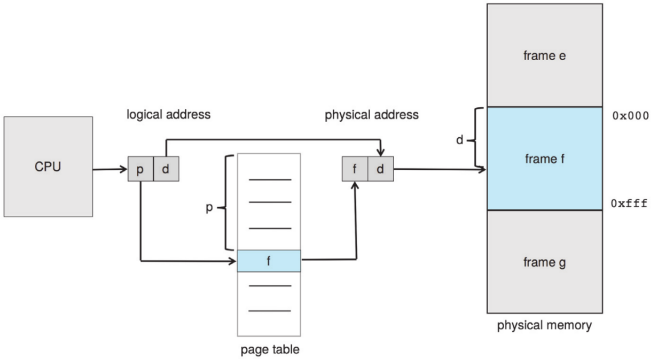
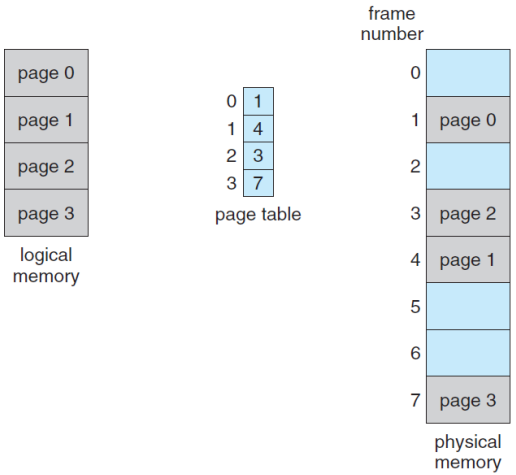
- For given logical address space 2^m and page size 2^n.

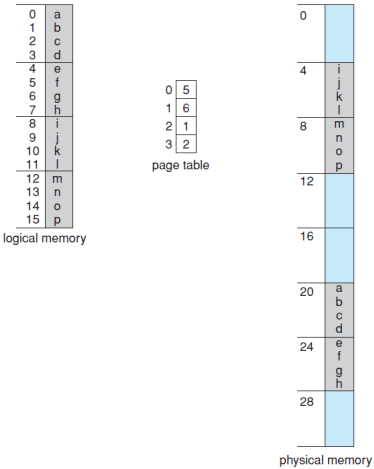
Paging Hardware



Paging Model of Logical and Physical Memory



Paging Example



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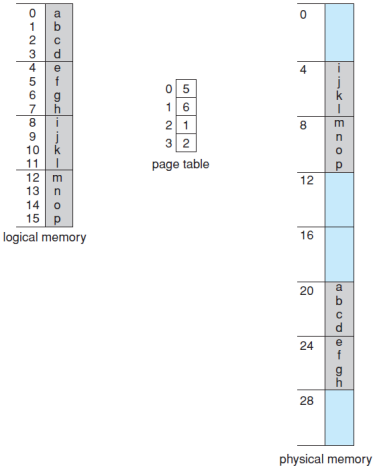

- The logical address:

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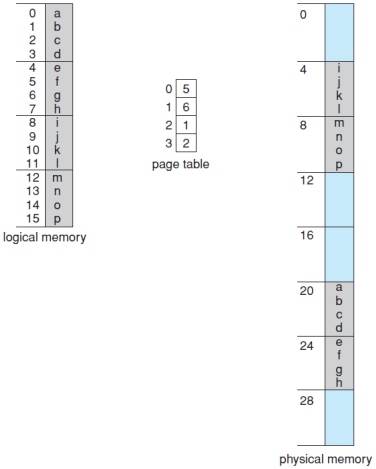
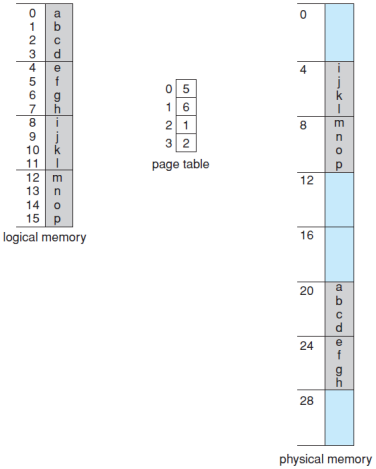


- The logical address: $m = 4$ and $n = 2$

Paging Example



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- Logical address 3:

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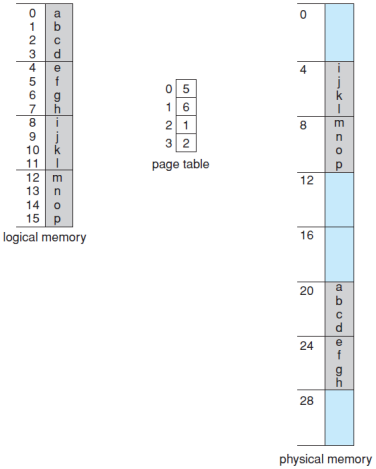
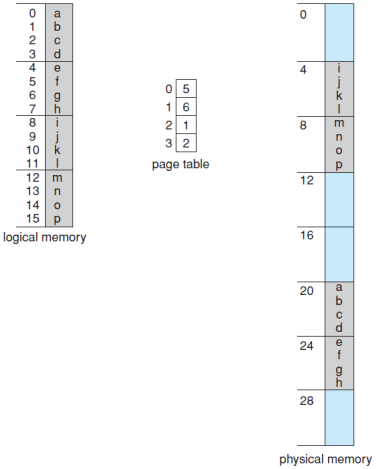


- The logical address: $m = 4$ and $n = 2$
- Logical address 3: $5 \times 4 + 3 = 23$

Paging Example



- The logical address: $m = 4$ and $n = 2$
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- Logical address 10:

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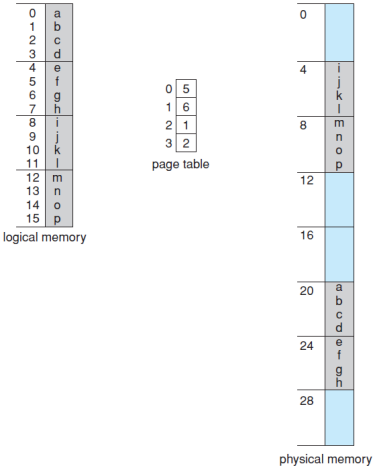

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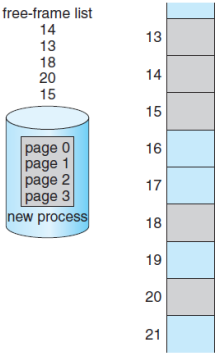
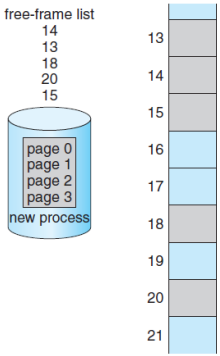
- Logical address 3: $5 \times 4 + 3 = 23$
- Logical address 10: $1 \times 4 + 2 = 6$

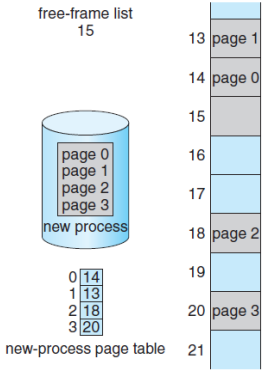
Free Frames


free-frame list
14
13
18
20
15
page 0
page 1
page 2
page 3
new process
13
14
15
16
17
18
19
20
21

Free Frames



before allocation



after allocation

Paging Example - Internal Fragmentation

- Page size = 2048 bytes
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- On average fragmentation = $\frac{1}{2}$ frame size

Small Page Size vs. Big Page Size

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- Small pages, more overhead is in the page-table, this overhead is reduced as the size of the pages increases.
- Disk I/O is more efficient when the amount data being transferred is larger (e.g., big pages).
- Pages typically are between 4 KB and 8 KB in size.

```
getconf PAGESIZE
```

Page Table Implementation

Page Table

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- Page-table base register (PTBR) points to the page table.
- Page-table length register (PTLR) indicates size of the page table.
- In this scheme every data/instruction access requires two memory accesses.
  - One for the page table and one for the data/instruction.

Translation Look-aside Buffers (1/2)

- The two memory access problem can be solved by the use of a special fast-lookup hardware cache called translation look-aside buffers (TLBs).

Translation Look-aside Buffers (2/2)

- TLB

Page #	Frame #

Translation Look-aside Buffers (2/2)

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Page #	Frame #

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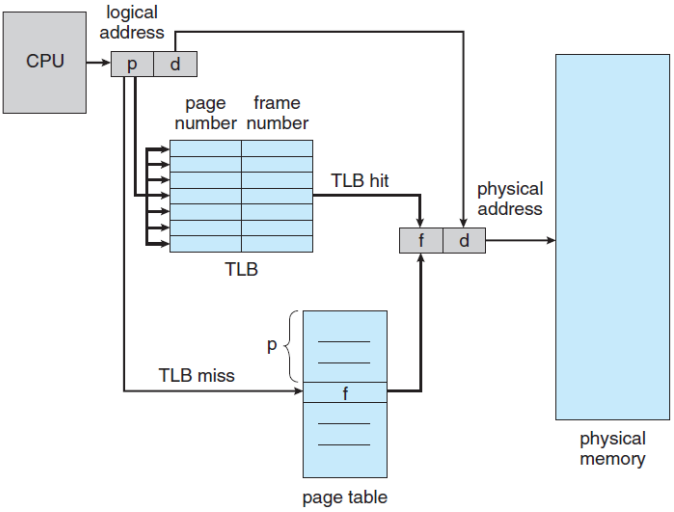
  - Otherwise, get *frame#* from page table.

Paging Hardware With TLB



Shared Pages

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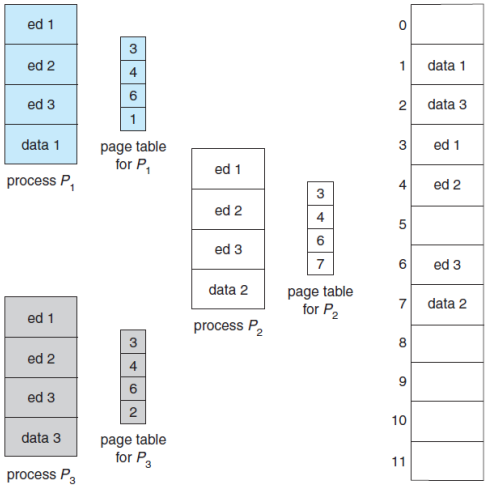
  - Similar to multiple threads sharing the same process space.
- Private code and data
  - Each process keeps a separate copy of the code and data.

Shared Pages Example



Structure of the Page Table

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  - That amount of memory used to cost a lot.
  - Don't want to allocate that contiguously in main memory.

Structure of the Page Table (2/2)

- Hashed Page Tables
- Hierarchical Paging

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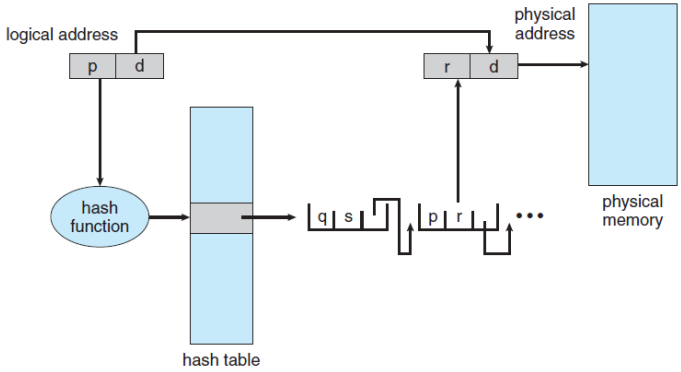
  2. The value of the mapped page frame
  3. A pointer to the next element

Hashed Page Table Architecture



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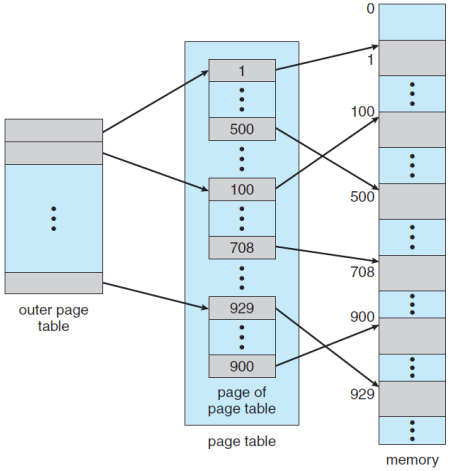
- A simple technique is a two-level page table.
- We then page the page table.

Two-Level Page-Table Scheme



Two-Level Paging Example

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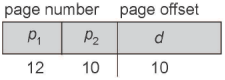

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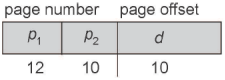

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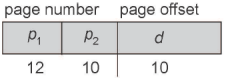
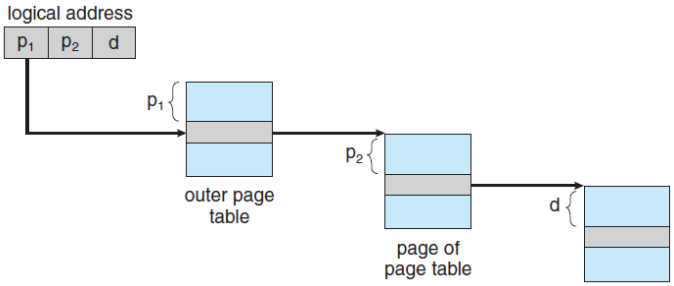


- p_1 is an index into the outer page table, and p_2 is the displacement within the page of the inner page table.
- Known as forward-mapped page table.

Address-Translation Scheme



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- Physical memory: frames, Logical memory: pages
- Page table: translates logical to physical addresses
- Translation Look-aside Buffer (TLB)
- Page table structure: hierarchical paging, hashed page tables

Questions?

Acknowledgements

Some slides were derived from Avi Silberschatz slides.