Memory Managment - Part I

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- The CPU fetches instructions from memory according to the value of the program counter.

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- Cache sits between main memory and registers.

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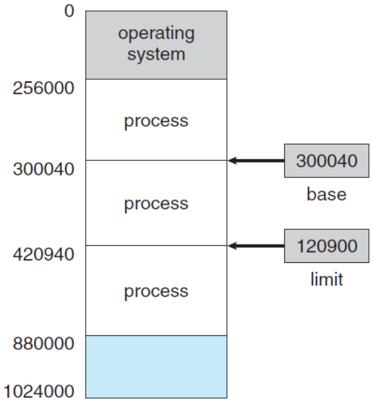
- A separate memory space for each process.
  - Determining the range of legal addresses that the process may access.

Base and Limit Registers

- A pair of base and limit registers define the logical address space.



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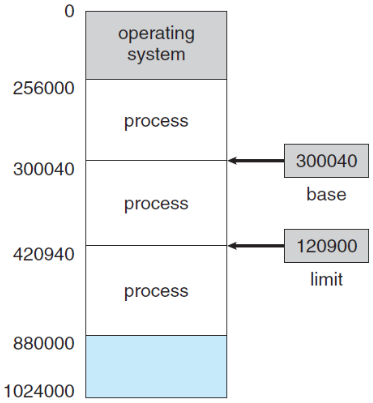
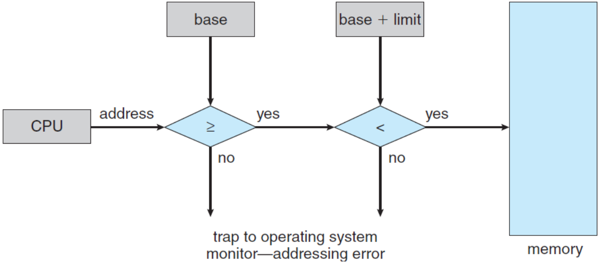
- CPU must check every memory access generated in user mode to be sure it is between base and limit for that user.



Hardware Address Protection

- Any attempt by a user program to access OS memory or other users' memory results in a trap to the OS, which treats the attempt as a fatal error.



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- A user process can reside in any part of the physical memory.

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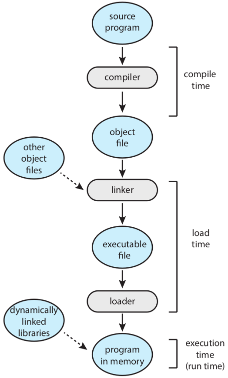

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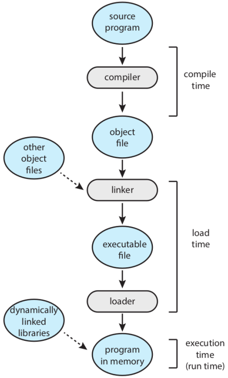

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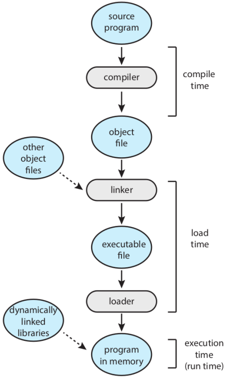

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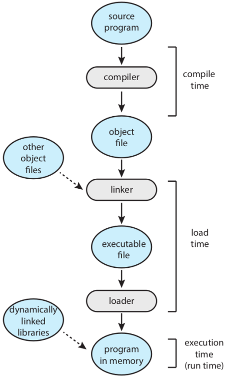

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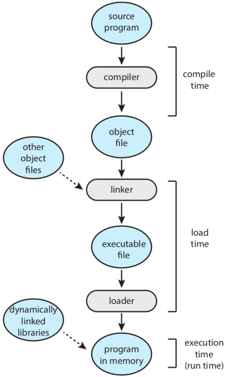

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- Load time: must generate relocatable code if memory location is not known at compile time.
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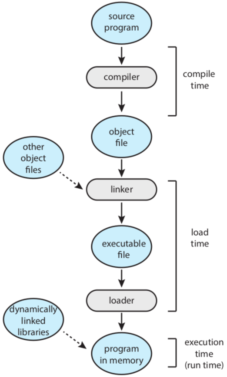
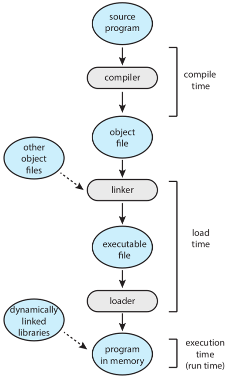
  - If the starting address changes, we need only reload the user code to incorporate this changed value.



Binding of Instructions and Data to Memory (3/3)

- Execution time: binding delayed until run time if the process can be moved during its execution from one memory segment to another.
    - Need hardware support



Logical vs. Physical Address Space

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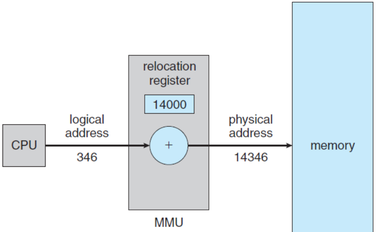

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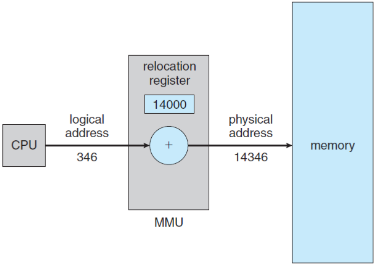
  - Base register now called relocation register.



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- Two different types of addresses:
  - Logical addresses: range 0 to max
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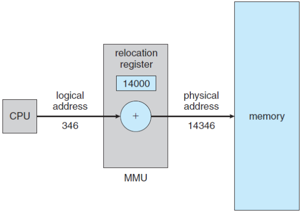

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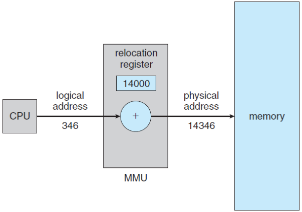

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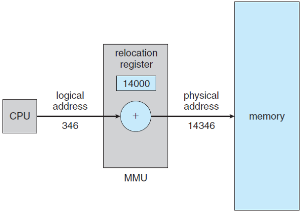
- These logical addresses must be mapped to physical addresses before they are used.



Dynamic Loading and Linking

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- Then control is passed to the newly loaded routine.

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- OS can help by providing libraries to implement dynamic loading.

Dynamic Linking

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  - Useful for shared libraries.

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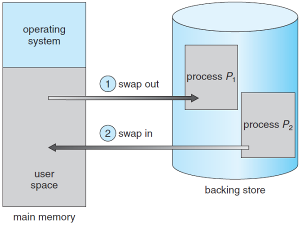
- Backing store: fast disk large enough to accommodate copies of all memory images for all users.



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- Example:
  - 100MB process swapping to hard disk with transfer rate of 50MB/sec.
  - Swap out time of 2s + swap in of same sized process.
  - Total context switch swapping component time of 4s.

Swapping on Mobile Systems (1/2)

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- Flash memory based
  - Small amount of space
  - Limited number of write cycles
  - Poor throughput between flash memory and CPU on mobile platform

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- Android terminates apps if low free memory, but first writes application state to flash for fast restart.

Contiguous Memory Allocation

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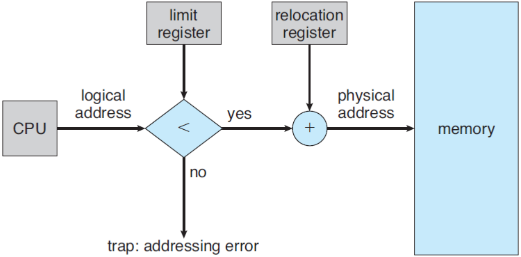
- Main memory usually into two partitions:
  - Resident OS and user processes memory address.
  - Each process contained in single contiguous section of memory.

Contiguous Allocation (2/2)

- Relocation registers used to protect user processes from each other, and from changing OS code and data.



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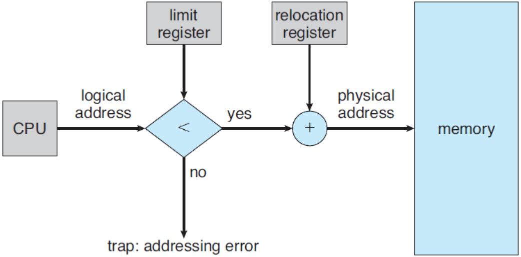

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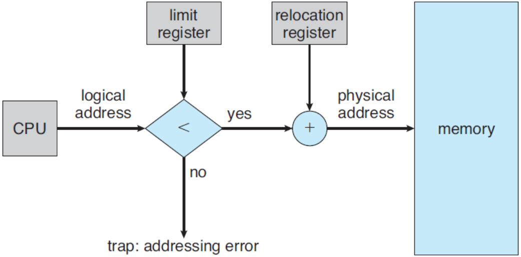

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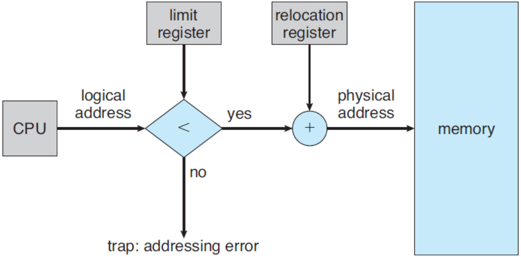
  - MMU maps logical address dynamically.



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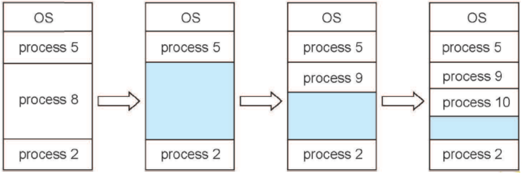

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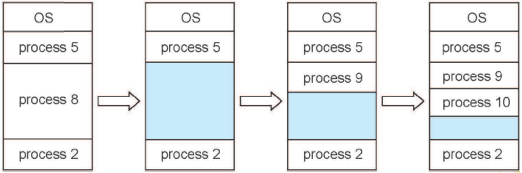

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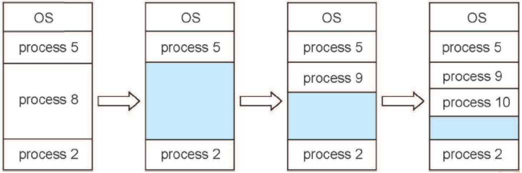

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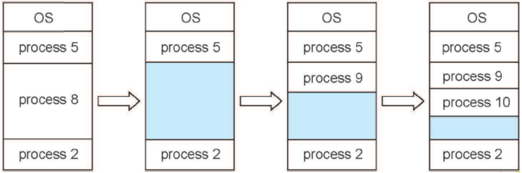

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- OS maintains information about: allocated partitions and free partitions (holes).

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- First-fit and best-fit better than worst-fit in terms of speed and storage utilization.

Fragmentation

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- Internal fragmentation: allocated memory may be slightly larger than requested memory; this size difference is memory internal to a partition, but not being used.

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- Two techniques:
  - Segmentation
  - Paging

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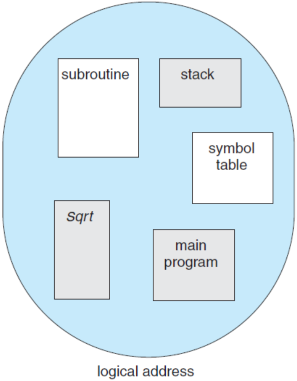

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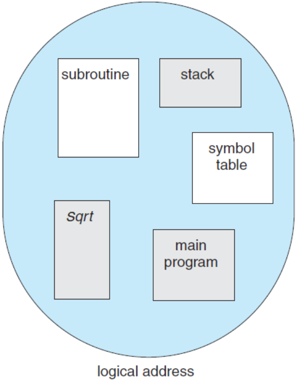

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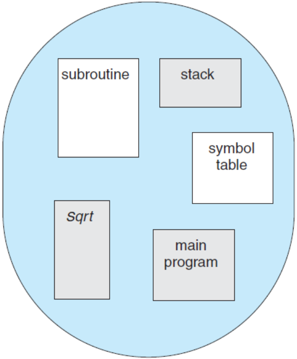
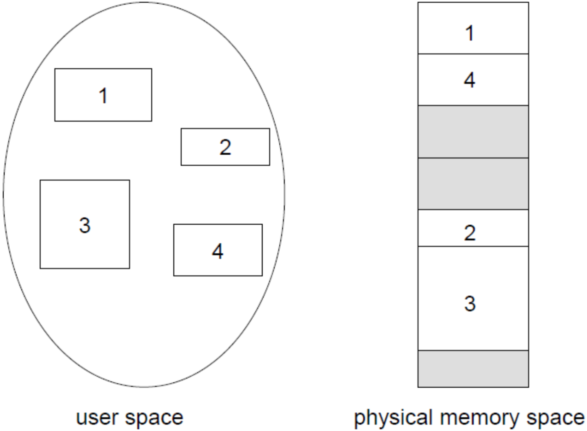
- A segment is a logical unit such as:
  - Main program
  - Procedure
  - Function
  - Object
  - ...



logical address

Logical View of Segmentation



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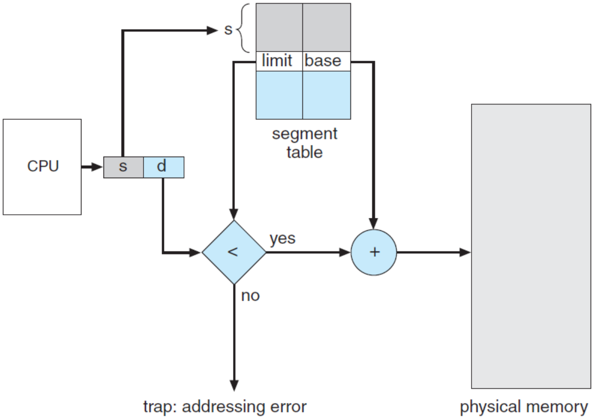
- Segment table: maps two-dimensional user-defined addresses into one-dimensional physical address.
- Each table entry has:
  - Base: contains the starting physical address where the segments reside in memory.
  - Limit: specifies the length of the segment.

Segmentation Hardware



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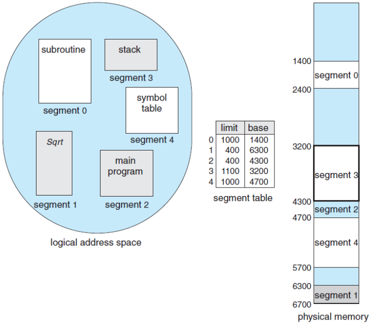

	limit	base
0	1000	1400
1	400	6300
2	400	4300
3	1100	3200
4	1000	4700

- A reference to byte 53 of segment 2:

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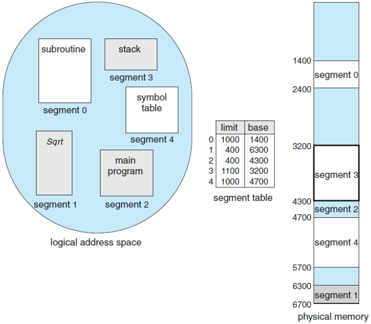

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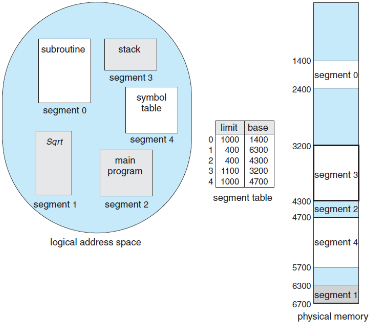
segment table

- A reference to byte 53 of segment 2: $4300 + 53 = 4353$

Segmentation Example

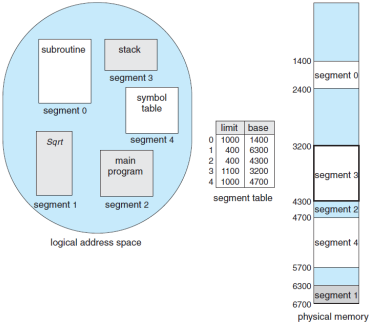


	limit	base
0	1000	1400
1	400	6300
2	400	4300
3	1100	3200
4	1000	4700

segment table

- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- A reference to byte 852 of segment 3:

Segmentation Example



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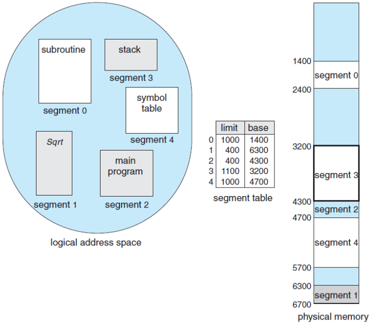
segment table

- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- A reference to byte 852 of segment 3: $3200 + 852 = 4052$

Segmentation Example



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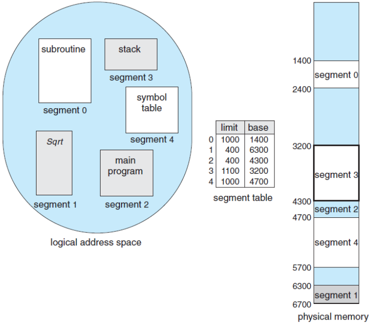
- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- A reference to byte 852 of segment 3: $3200 + 852 = 4052$
- A reference to byte 1222 of segment 0:

Segmentation Example



	limit	base
0	1000	1400
1	400	6300
2	400	4300
3	1100	3200
4	1000	4700

- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- A reference to byte 852 of segment 3: $3200 + 852 = 4052$
- A reference to byte 1222 of segment 0: trap to OS

Summary

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- External and internal fragmentation: compaction, segmentation, paging
- Segmentation: noncontiguous address, user view of memory

Questions?

Acknowledgements

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